

規格書

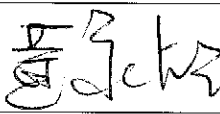

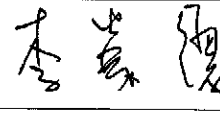
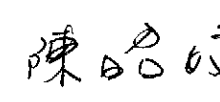
SPECIFICATION

品名
STYLE NAME : REDUNDANT SWITCHING POWER SUPPLY

型號
MODEL NO. : G1W2-5760V3V

料號
PART NO. :

版次
REVISION : A1

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Revision

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1.0 Scope

This specification defines the performance characteristics of a grounded , single-phase , 760 watts , 5 output level power supply. This specification also defines world wide safety requirements and manufactures process test requirements.

G1W2-5760V3V power system is a 1+1 Redundant power system consisting of two G1W-3760V power modules and one G1W2-5760V3V power system frame.

2.0 Input requirements

2.1 Voltage (sinusoidal)

Full range 100~240 VAC (With $\pm 10\%$ tolerance)

2.2 Frequency

The input frequency range will be 50Hz/60Hz(± 3 Hz).

2.3 Steady-state current

11.0 – 5.5 amps maximum at any low/high range input voltage.

2.4 Inrush current

60 / 80 amps @115/230 VAC (at 25 degrees ambient cold start for each power unit)

2.5 Power factor correction

The power supply modules shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the EN 61000-3-2 standards.

PFC can reach the target of 95% @115V,full load.

3.0 Output requirements

3.1 DC load requirements

Normal Output voltage	Load current		Regulation tolerance	
	Max.	Min	Max.	Min.
+5V	32.0	0.5	+5%	-5%
+12V	62.0	2.0	+5%	-5%
-12V	0.8	0.0	+10%	-10%
+3.3V	32.0	0.5	+5%	-5%
+5VSB	3.5	0.1	+5%	-5%

*** +5V and +3.3V total output max : 190W ***

*** Total output max : 760W ***

When doing the cross regulation test(one output channel at high load and the other output channels at low load), it is requested to set the higher output channel at 80% max. of its spec., and the lower output channels at 20% max. of theirs.

3.2 Regulation

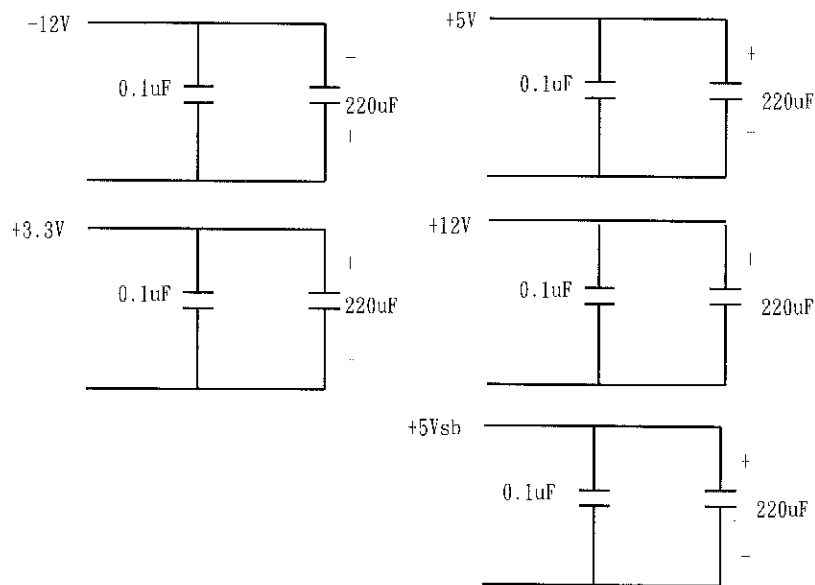
Output DC voltage	Line regulation
+5V	± 50 mV
+12V	± 120 mV
-12V	± 120 mV
+3.3V	± 50 mV
+5VSB	± 50 mV

3.3 Ripple and noise

3.3.1 Specification

+5V	50mV (P-P)
+12V	120mV (P-P)
-12V	120mV (P-P)
+3.3V	50mV (P-P)
+5VSB	50mV (P-P)

3.3.2 Ripple voltage test circuit



0.1uF is ceramic, the other is electrolytic capacitor.
Noise bandwidth is from DC to 20Mhz

3.4 Overshoot

Any overshoot at turn on or turn off shall be less than 10% of the nominal voltage value , all output shall be within the regulation limit of section 3.1 before issuing the power good signal of section 6.0.

3.5 Efficiency

Power supply efficiency typical >80% at 230V full load .

P.S:

Any difference either on the DC output cable (i.e., length, wire gauge) or on the accurate of instruments will conclude different test result.

3.6 Remote on/off control

The power supply DC outputs (with the exception of +5VSB) shall be enabled with an active-low , TTL-compatible signal(“PS-ON”)

When PS-ON is pulled to TTL low , the DC outputs are to be enabled.

When PS-ON is pulled to TTL high or open circuited , the DC outputs are to be disabled.

4.0 Protection

4.1 Input (primary)

The input power line must have an over power protection device in accordance with safety requirement of section 8.0

4.2 Output (secondary)

4.2.1 Over power protection (one unit)

The power supply shall provide over power protection on the power supply latches all DC output into a shutdown state. Over power of this type shall cause no damage to power supply , after over load is removed and a power on/off cycle is initiated , the power supply will restart.

Trip point total power min. 110% , max. 150%.

4.2.2 Over voltage protection

If an over voltage fault occurs , the power supply will latch all DC output into a shutdown state before

+5V : 5.7V ~ 6.2V

+3.3V : 3.7V ~ 4.1V

+12V : 13.3V ~ 14.3V

4.2.3 Short circuit

A: A short circuit placed on any DC output to DC return shall cause no damage.

B: The power supply shall be latched in case any short circuit is taken place at +5V,+3.3V,+12V,-12V output.

C: The power supply shall be auto-recovered in case any short circuit is taken place at +5VSB.

4.2.4 Over current protection

If an over current fault occurs , the power supply will latch all DC output into a shutdown state.

	Min	Typical	Max
+3.3V	35A	42A	48A
+5V	35A	42A	48A
+12V	68A	81A	93A

5.0 Power supply sequencing

5.1 Power on (sec fig.1)

5.2 Hold up time

When power shutdown DC output 5V must be maintain 16msec in regulation limit at normal input voltage.

5.3 Power off sequence (sec fig. 1)

6.0 Signal requirements

6.1 Power good signal (see fig. 1)

The power supply shall provide a "power good" signal to reset system logic & indicate proper operation of the power supply.

At power on & the power good signal shall have a turn on delay of at least 100ms but not greater than 500ms after the output voltages have reached their respective minimum sense levels.

7.0 Environment

7.1 Temperature

Operating temperature	0 to 40 degrees centigrade
Non-Operating temperature	-20 to 80 degrees centigrade

7.2 Humidity

Operating humidity	20% to 80%
Non-operating humidity	10% to 90%

7.3 Insulation resistance

Primary to secondary	: 100 meg. ohm min. 500 VDC
Primary to Frame Gnd	: 100 meg. ohm min. 500 VDC

7.4 Dielectric withstanding voltage

For approval purpose :

Primary to secondary	: 3KVAC for 1min.
Primary to Frame Gnd	: 1500 VAC for 1 min.

For production purpose: 100% test

Primary to Frame Gnd	: 1800VAC for 2 sec
Cut off current	15mA

7.5 Leakage current

3.5 mA. max. at nominal voltage 250 VAC

8.0 Safety

8.1 Recognized to U.S. and Canadian requirements under the component recognition program of Underwriters Laboratories Inc.

The power supply shall be designed to meet UL60950.

8.2 TUV Standards

The power supply shall be designed to meet TUV EN-60950.

8.3 CB

The power supply shall be designed to meet CB IEC 60950.

9.0 Reliability

9.1 Burn in

All products shipped to customer must be processed by burn-in. The burn-in shall be performed for 1 hour at full load.

10.0 Mechanical requirements

Physical dimension : 300 mm * 101.2 mm * 84 mm (D*W*H)

11.0 Warning method

11.1 Audio alarm(buzzer sound,resetable)

11.2 Fault LED

11.3 Power defective signal delivery(TTL,Lowactive)

12.0 DC output cable drawing

(see attached drawing)

13.0 Output voltage Timing

Item	Description	MIN	MAX	UNITS
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	16		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK.	15		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok_off	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
Tsb_vout	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	5	1000	ms
Tsb_holdup	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms
Tvout_rise	Output voltage rise time from each main output.	5	20	ms

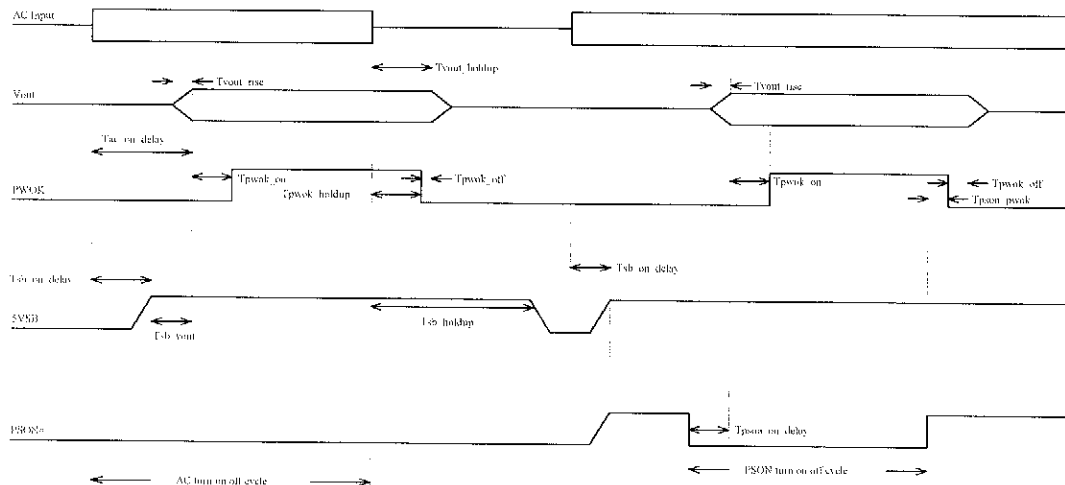


Fig.1